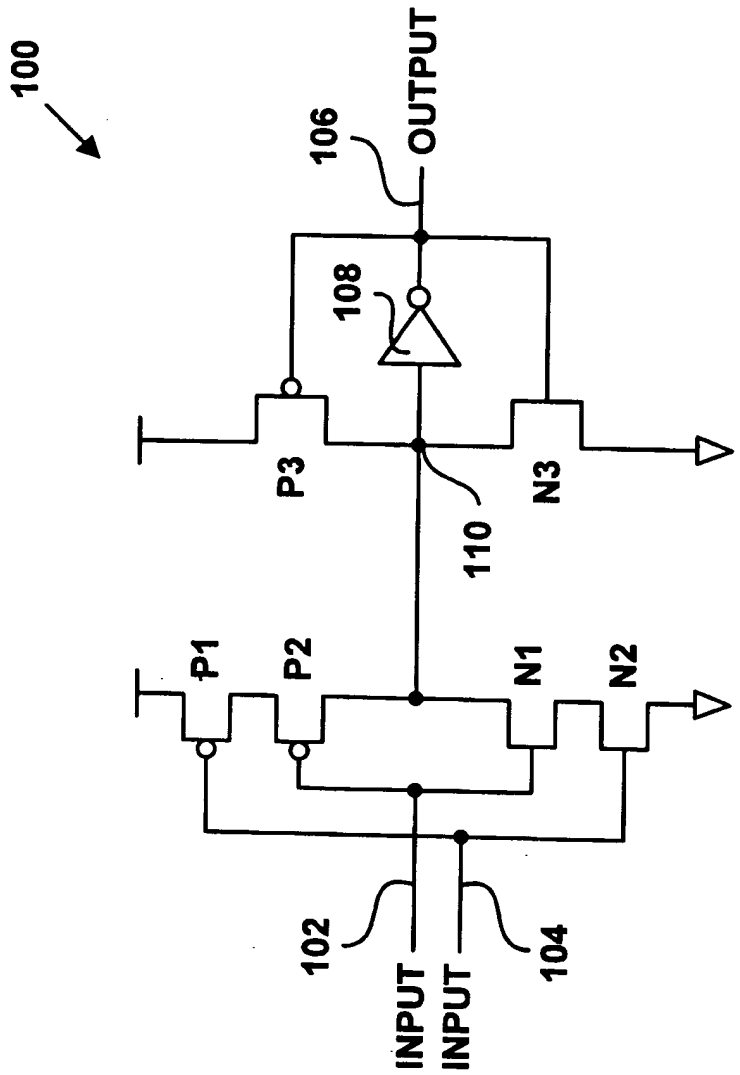

Fig. 1

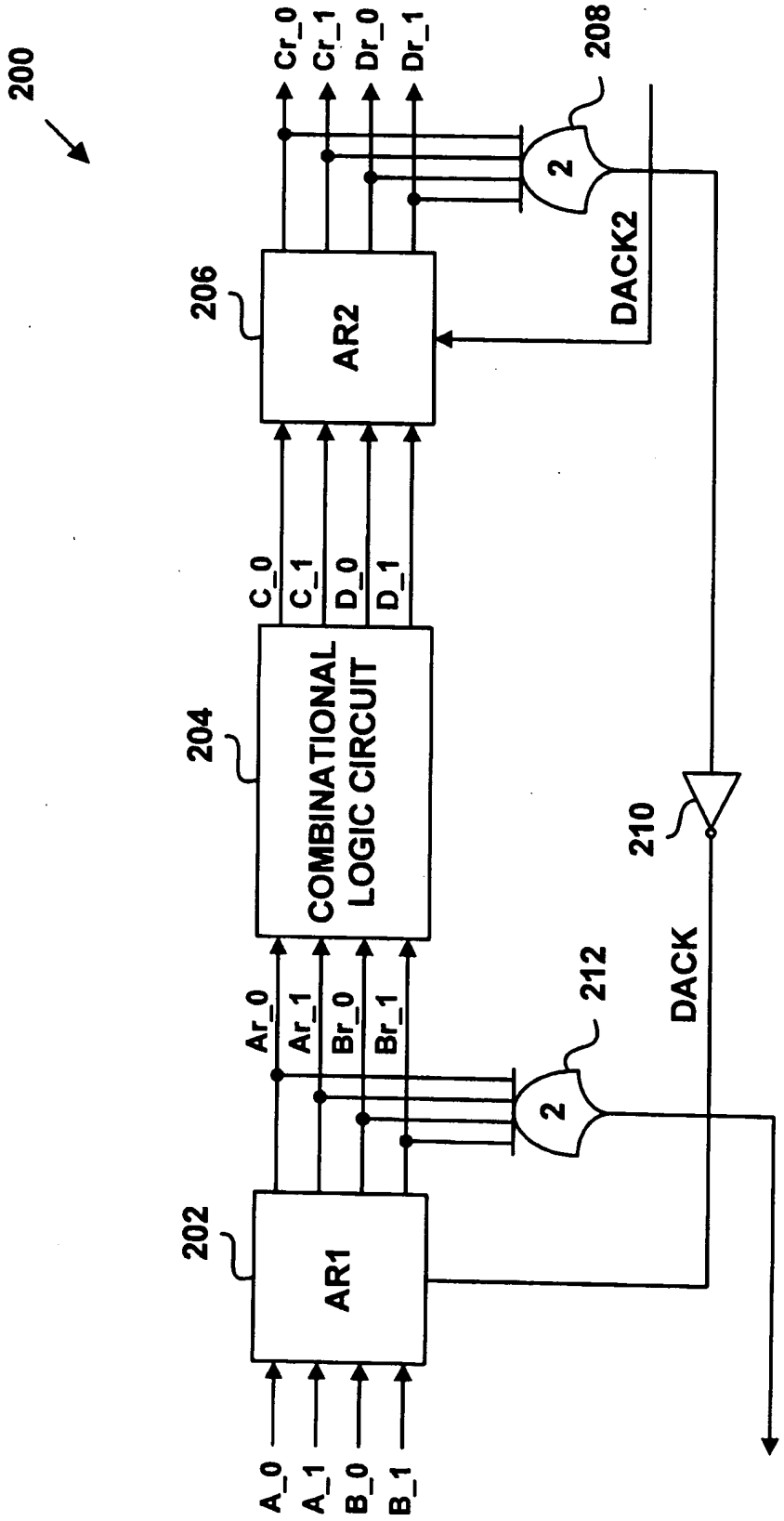
200
Cr_0
Cr_1
Dr_0
Dr_1
208
2
DACK2
206
AR2
C_0
C_1
D_0
D_1
204
COMBINATIONAL LOGIC CIRCUIT
210
Ar_0
Ar_1
Br_0
Br_1
212
2
DACK
202
AR1
A_0
A_1
B_0
B_1

Fig. 2

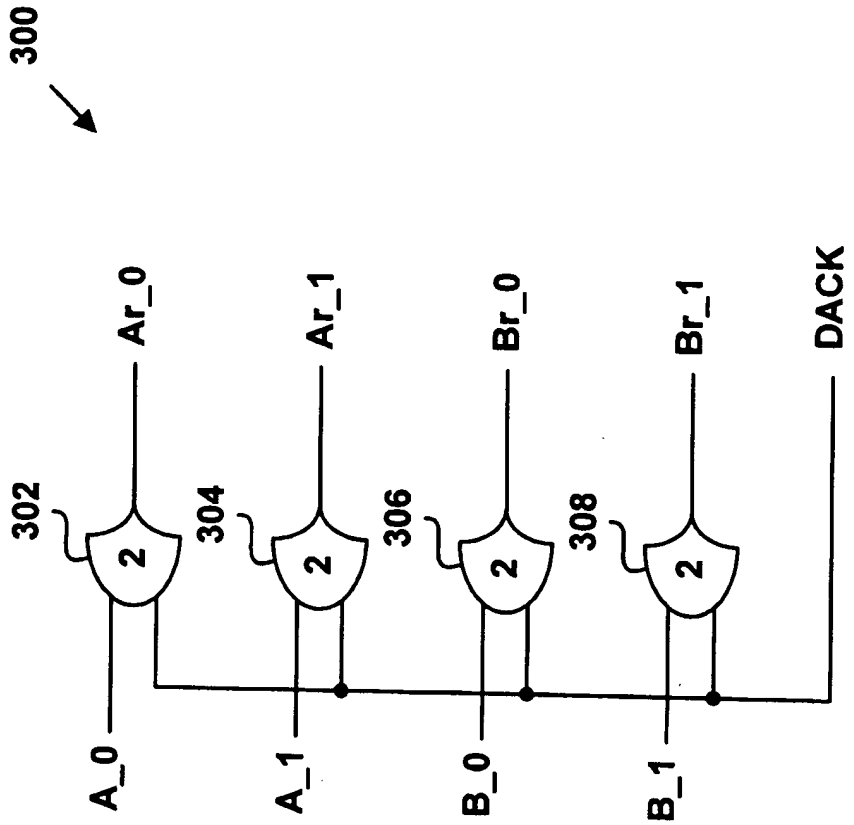

Fig. 3

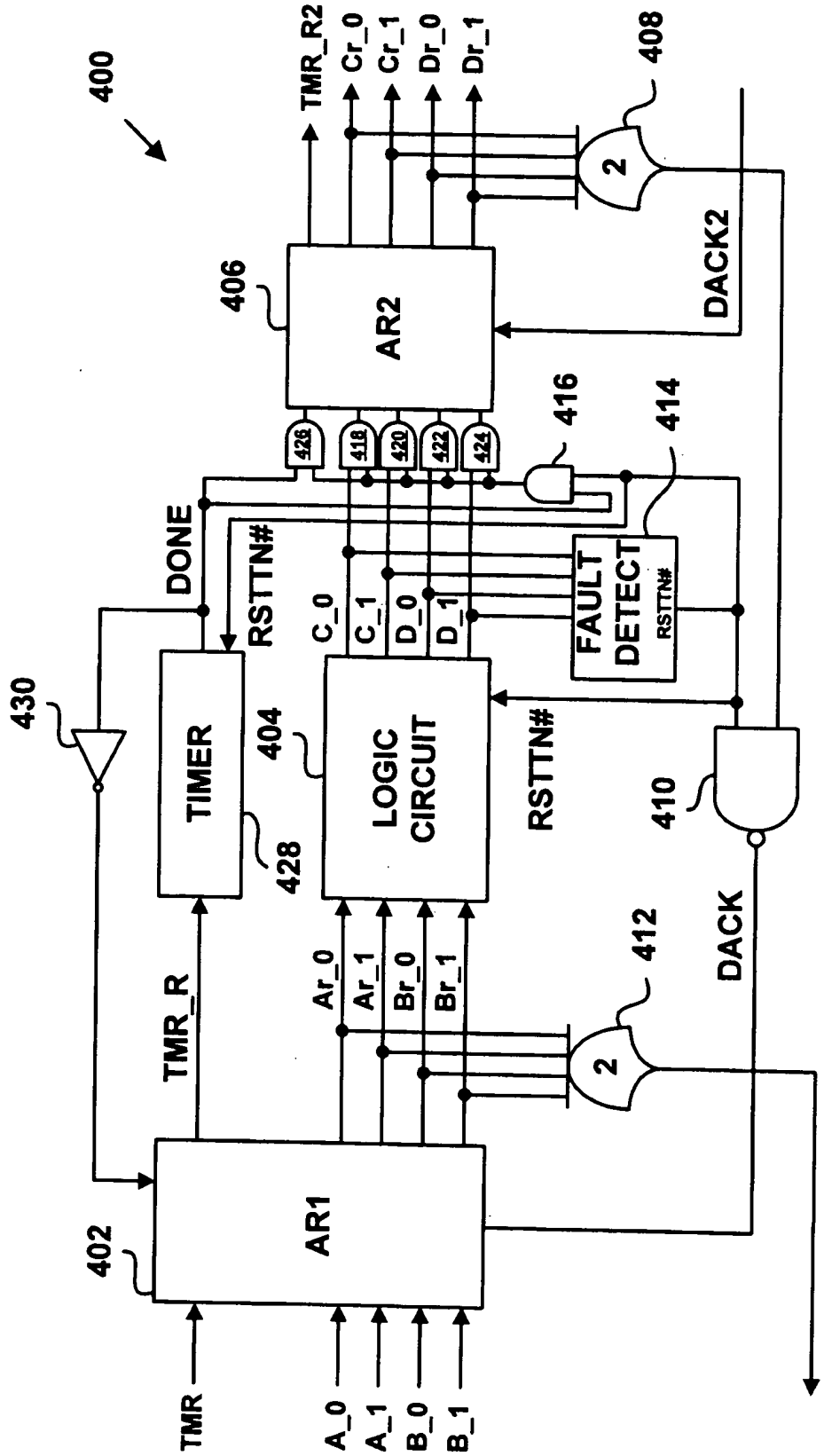
400
TMR_R2
Cr_0
Cr_1
Dr_0
Dr_1
408
2
DACK2
406
AR2
416
414
426
418
420
422
424
DONE
RSTTN#
C_0
C_1
D_0
D_1
FAULT DETECT
RSTTN#
430
TIMER
404
LOGIC CIRCUIT
RSTTN#
410
428
TMR_R
Ar_0
Ar_1
Br_0
Br_1
412
DACK
2
AR1
402
TMR
A_0
A_1
B_0
B_1

Fig. 4

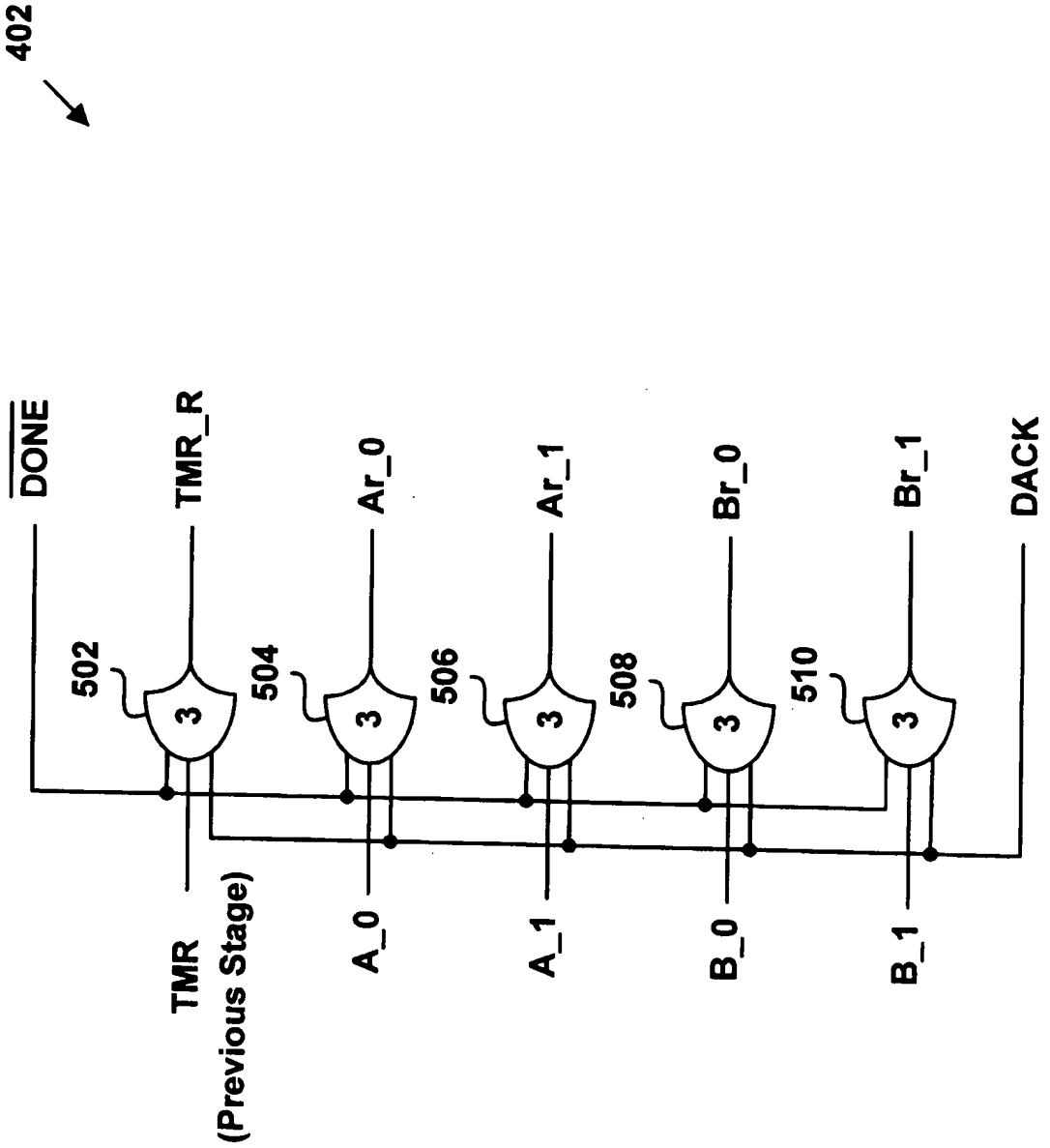
402
DONE
TMR_R
Ar_0
Ar_1
Br_0
Br_1
DACK
502
504
506
508
510
3
3
3
3
3
TMR
(Previous Stage)
A_0
A_1
B_0
B_1

Fig. 5

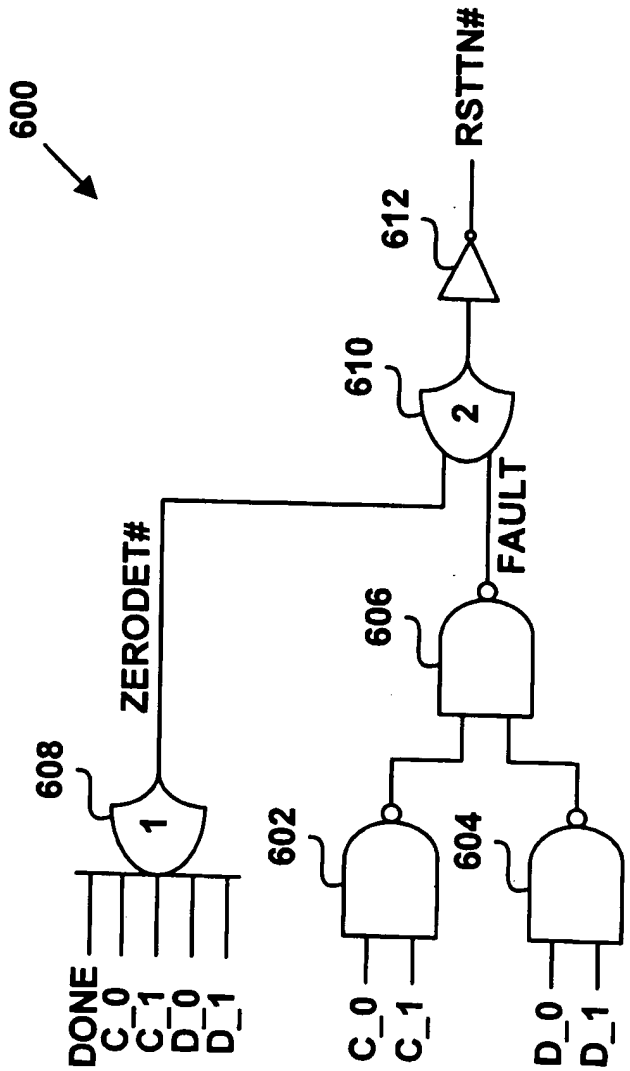
600
RSTTN#
612
610
2
FAULT
606
ZERODET#
608
1
602
604
DONE
C_0
C_1
D_0
D_1
C_0
C_1
D_0
D_1

Fig. 6

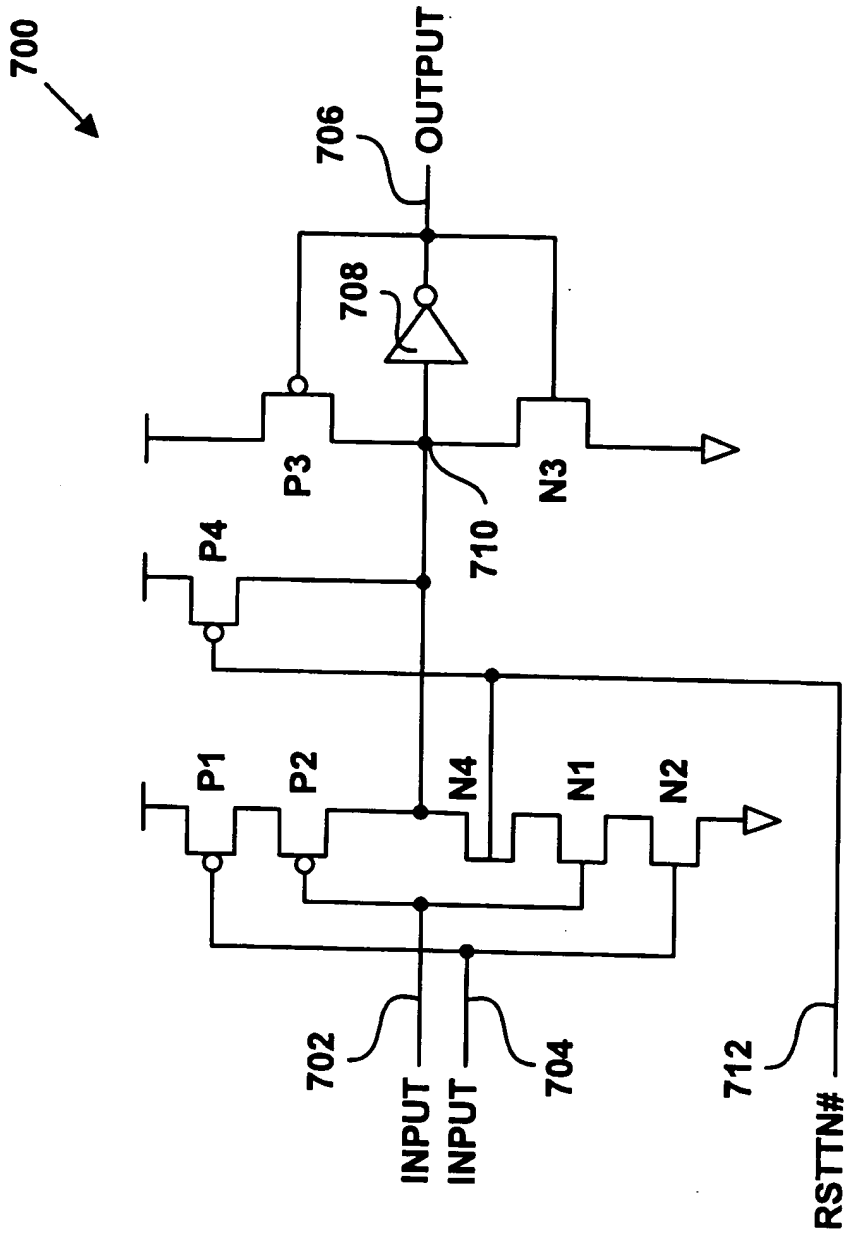
700
706
OUTPUT
708
P3
N3
710
P4
P1
P2
N4
N1
N2
702
704
712
INPUT
INPUT
RSTTN#

Fig. 7

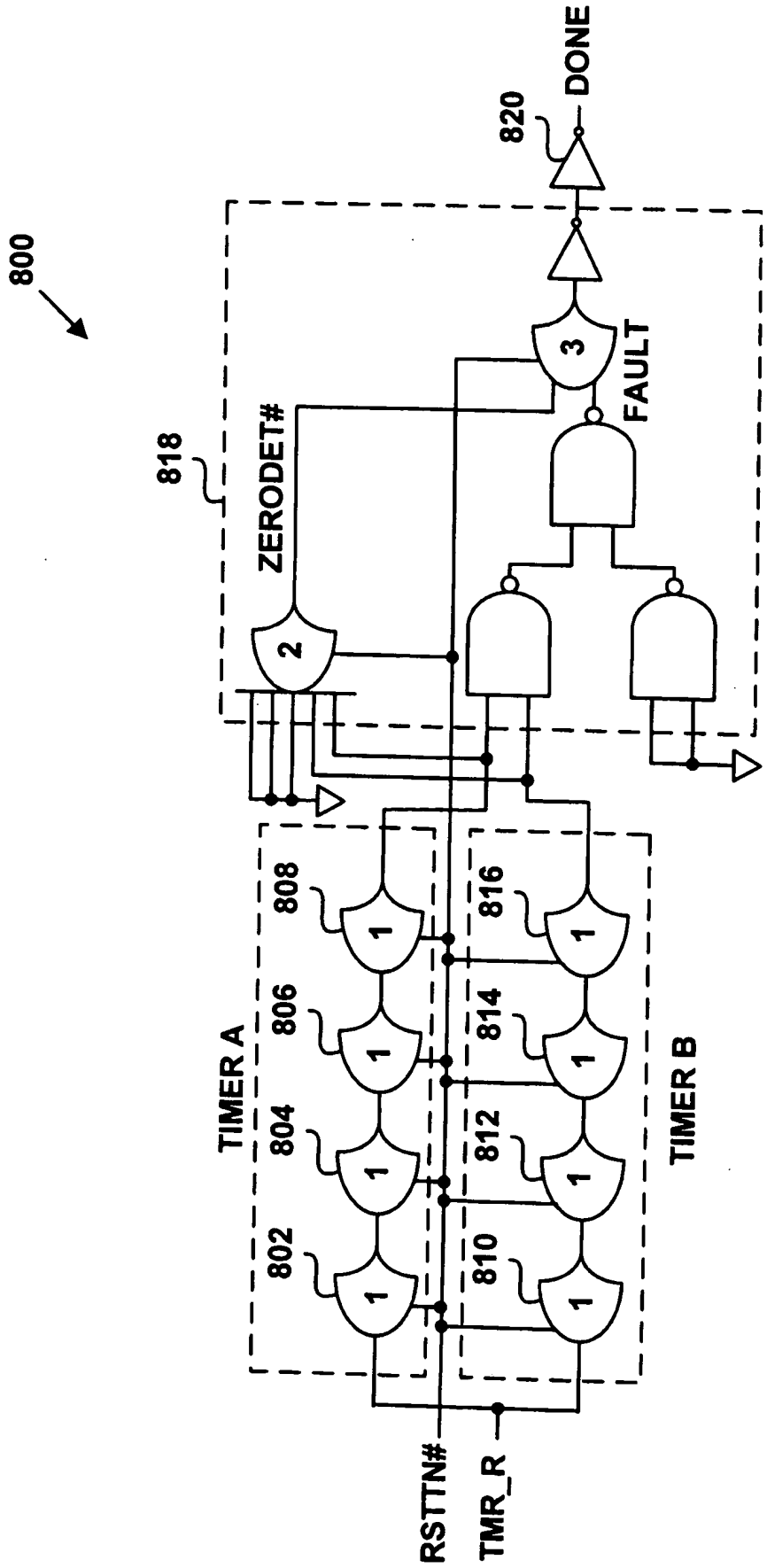
800
DONE
820
FAULT
3
ZERODET#
818
2
TIMER A
TIMER B
808
806
804
802
816
814
812
810
1
RSTTN#
TMR_R

Fig. 8